Jie Gao

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LinkedIn: link

Education		
Rice University	Houston, Texas	08/2022-08/2024 (expected)
Master of Electrical and Computer Engineering		
University of Mississippi	Oxford, Mississippi	08/2019 - 06/2022
Bachelor of Science in Electrical and Computer En	ngineering	
Current GPA: 3.60/4.00 (Cum Laude)		
Skills		
Hardware: FPGA (Xilinx Nexys 7, Zynq 7000) and	nd MCU (STM32, 8051, etc.)
Development Environment: Vivado, Vitis, Matla	b Simulink, Multisim, LTspi	ce, and Keil5.
Computer-Aided Design Software: Visio, Kicad,	and AutoCAD.	
Coding Skills: VHDL & Verilog HDL, MATLAB	, C, Python, System Verilog	, and Shell.
Relevant Experience		
Build a 4x4 Matrix Multiplier Using Xilinx HLS	5 Tools, Rice University, Ho	ouston 09/2022-10/2022
*Used the adder, multiplier, and Mux modules with	h the Matlab Simulink modu	le provided by Xilinx (Model
Compressor) to build a 4x4 matrix multiplier.		
*Simulated the design and obtained the delay and n output through MATLAB	resource usage results, and pr	cocess the results of the matrix
*Co-simulated the design on the FPGA (Via JTAG	i).	
A TENS skin stimulator for testing a tactical fee	edback stuttering prosthetic	c in an MRI(Senior Design) 08/2021 - 06/2022
*Design and developed a device that can help stutt	er patients overcome stuttering	ng through electrical stimulation
with a team of there. It was designed and complete	d by me and two other stude	nts.
*Completed the schematic diagram of the whole pr	roject,	
*Finished the design of the PCB board, with Kicad	(the final design is a 3-layer	PCB board), programming with
Arduno to control the DS1803 digital potentiomet	er.	
Automatic obstacle avoidance car based on S1N	132, University of Mississip	11/2021 - 12/2021
*Dised the ultrasonic ranging sensor, STM32 devel	opment board, keyboard, and	i stepper motor.
According to the course requirements STM32 CL	BE was not used	ging the value of the registers.
*Collaborate with a group of four	BE was not used.	
Digital IC Verification Engineer Intern TONG	XIN MICRO Beijing	06/2021 - 08/2021
*Performed regression testing on the UVM test pla	tform tested functional cove	erage and wrote test documents
* Verified the module design On the Xilinx Zyna-	7000 FPGA and reported the	problem to the superior.
*Wrote testbench based on System Verilog.		processi to the superior.
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Publication		
Jie Gao, Shaotong Li, Yiding Ma, & Zhao Zhang,	(2021). The Methods for Hig	gh-Speed Low-Power Dynamic ADC
Comparators Design (English). The 2021 IEEE Int	ternational Conference on El	ectronic Information Engineering
and Computer Science (IEEE-EIECS 2021). Change	gchun, China. Accepted and	in press.
Relevant Awards		
Changellen's Hener will in 2022 Service Serverter	University of Mississi	05/2022

Chancellor's Honor roll in 2022 Spring Semester	University of Mississippi	05/2022
Dean's Excellence Award in Engineering	University of Mississippi	04/2022
Dean's Honor Roll in 2021 Fall semester	University of Mississippi	12/2021