Xinyi Qi

xq14@rice.edu

EDUCATION

Rice University, *Houston, TX* Dec. 2022
Master in Electrical and Computer Engineering
Shanghai Jiao Tong University, *Shanghai, China* Aug. 2020
University of Michigan - Shanghai Jiao Tong University Joint Institute
Bachelor of Science in Electrical and Computer Engineering
• **GPA:** 3.54/4.00 **Major GPA:** 3.71/4.00
• **Courses:** *Advanced Digital IC design, Advanced VLSI Design, High-performance Computer Architecture, Operating System and Concurrent Programming, Digital Signal Processing, Introduction to Data Structures*

PROJECT EXPERIENCE

In-Memory Computing XNOR SRAM Nov. 2021 - present
• Implemented the XNOR SRAM bitcell in Cadence Virtuoso, test its XNOR functional behavior under different input conditions
• Optimized the PMOS sizing for the Pull-up and Pull-down logic inside the bitcell for a better delay performance
• Building a 4-by-4 SRAM system to test the XNOR and Accumulation functions under different process corners

High-performance Hardware Implementation of ECC Encryption Algorithm Jun. 2021 - Aug. 2021
• Designed the SHA1 module in Verilog to produce a 160-bit summary of input plaintext
• Implemented Montgomery algorithm to accelerate the modular multiplication, and wrote C prototype to do functional verification
• Analyzed the modular multiplication module's side-channel-attack resistance and proposed algorithm-level countermeasures

Pipelined Implementation of MIPS Computer Jul. 2019 - Aug. 2019
• Designed pipeline architecture diagram and handled hazards by designing forwarding unit and hazard-detecting unit
• Implemented logic blocks in Verilog and combined them according to the architecture diagram
• Held functional verification in Vivado and FPGA board-level verification with various MIPS test programs

8-bit Multiplier Optimization Sep. 2018 - Oct. 2018
• Created circuit schematics of the 8-bit multiplier in Cadence Virtuoso, simulated, and calculated the energy-delay product before and after my optimization
• Replaced ordinary adders with carry-lookahead adders to improve the calculation speed
• Reduced the energy-delay product by 34%

RESEARCH EXPERIENCE

Systolic-array based Matrix Multiplication RISC-V Accelerator Sep. 2021 - present
• Built the systolic-array schematic through Vitis HLS in C++, pipelined the structure with pragma
• Simulated the design in Vivado, and analyzed the performance and resource utilization
• Learning Chisel HDL to implement the systolic-array core and tightly coupled it with a RISC-V Rocket core through the RoCC interface

WORK EXPERIENCE

Pixelworks, Digital IC Design Intern, *Shanghai, China* Apr. 2021 – Jul. 2021
• Ran CDC (Clock Domain Crossing) checks for IPs, went through the RTL design code to locate violation reasons, and wrote corresponding waive scripts using TCL
• Wrote Perl scripts to run automatic CDC check for certain IPs and generate post-processed versions of reports for the back-end teams
• Draw the ECO concept diagram and updated design and functional specifications for IPs

SKILLS

• **Programming Language:** Verilog HDL, C, C++, Perl, TCL, Python, Objective-C
• **Software:** Questa CDC Verification, Xilinx Vivado, HSpice, Cadence Virtuoso, QuestaSim, , Matlab Simulink, VitisHLS
• **Language:** English, Mandarin
• **Other skills:** Linux command, Version control systems [git, svn]