Liwen Jiang

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EDUCATION

Rice University Aug 2020 - May 2022
Electrical Engineering, Master, GPA:4.0/4.0 Houston, TX
Honors/Awards: Lowenstern Fellowship(2020-2021)
Relevant Coursework: Advanced Digital IC Design, Wireless IC, Learning from Sensor Data

Rice University Aug 2016 - May 2020
Electrical Engineering, Bachelor of Science, GPA: 3.72/4.0 Houston, TX
Honors/Awards: Best Undergraduate Research Award(2019), NSF Award(2018), Rice ECE Bybee Travel and Research Award(2017-2018), President Honor Student(2017-2018)
Relevant Coursework: H-S System Design, Analog IC, VLSI Design, Digital Integrated Circuits, Digital Circuits, Electronic Materials, Signals and Systems, Digital Communication
Paper: Neural Network DPD via Backpropagation through a Neural Network Model of the PA

TECHNICAL SKILLS

Programming Languages: Verilog, Matlab, Python, C, C++, Bash, Html, Javascript, CSS
Software: Cscope, Cadence Virtuoso, Vivado, VirtualBench, Labview, Eagle, Encounter, H/LTSpice, Hyperlynx, Magic, ModelSim, OriginLab
Hardware: FPGA, Arduino, RaspberryPi, TI MSP430/TM4C123G LaunchPad
Instruments: NI DAQ Card, Multimeter, Oscilloscope, Sourcemeter, DC/AC Power Supply, Function Generator, Frequency Counter

PROFESSIONAL EXPERIENCE

Rice Secure and Intelligent Micro-Systems (SIMS) Lab May 2020 - Oct 2021
Research Assistant Houston, TX

- Designed a wirelessly powered and clocked mixed-signal sub-uW highly accurate CMOS smart integrated temperature sensor in the subthreshold region within Cadence Desgin Suit, taped out in TSMC 180nm Process.
- Lay outed circuits and performed post-layout simulation/optimization using Calibre. Wrote testbench in Verilog to test the pre/post-synthesis scan chain and readout circuits.
- Built and soldered testing PCB to validate chip performance inside the temperature chamber with NI DAQ Card using Labview, analyzing data in Python with Pandas and Numpy and visualizing with Matplotlib & Origin.
- Communicated with domestic/international suppliers/distributors to source testing equipment.

Cisco Systems Inc May 2019 - Aug 2019
Hardware Intern Cloud Network Group San Francisco, CA

- Designed and tested a LTE-enabled camera, utilizing a PLAS9-X module interacting with a APQ8053 chip to transmit/receive video signals over cellular network, awarded with a business trip to visit joint design manufacturers in Taiwan.
- Drew a 4-layer high speed PCB board with Cadence/Allegro PCB Designer based on the existent 8-layer-board product, sourcing components and communicating with the local PCB manufacturer to gerber out 15 pieces of design in a week.

OpenStax May 2017 - Aug 2017
Software Intern Front-end Department Houston, TX

- Improved user experience by creating additional navigation levels inside the existent table of contents based on Backbone model and Coffeescript.
- Independently involved in frontend development for a flip-card web app based on Html, CSS and Javascript, earning a $2000 bonus with team members for good performance of web app.

RESEARCH EXPERIENCE

Parallel Hardware Applications in Science and Technology Jan 2018 - Aug 2020
Undergraduate Research Assistant Rice PHAST Group Houston, TX

- Performed Digital Pre-distortion(DPD) with memory effects in a customized OFDM system by modelling the power amplifier with neural network in Matlab to reduce the oversampling ratio from 5 to 2 and created a GUI with Python Tkinter library to automate experiments and result presentation and published a paper at 2019 IEEE Asilomar Conference on Signals, Systems and Computers.

Autonomous Tetherless Networked Drone May 2018 - Aug 2018
Undergraduate Research Assistant Rice Network Group Houston, TX

- Wrote autonomous missions for measuring air quality, detecting transmitted signal strength and optimizing drones' flight path with flight data and recording videos/capturing images and successfully deployed on drones for field experiments.
- Collected data from gas sensors, IRIS/RTL SDR(radio frequency sensors) and motion sensors with Python based on GPIO Port of Raspberry Pi and UART Port of Arduino Nano and visualize the data by using the Matplotlib and Numpy libraries two weeks earlier than expected deadline.

PROJECT EXPERIENCE

UART ASIC Chip in MOSIS AMI 0.5 Micron Process Jan 2019 - May 2019

- Built and taped out a 40-pin-pad-frame communication chip that integrated a transmitter and a receiver, implementing the UART protocol in 6-stage FSM based on 2-phase clocking.
- Designed in Verilog and simulated in Modelsim, synthesizing the RTL design in Synopsys Design Compiler.
- Generated the layout with Encounter and translated into a Magic file, testing with Irsim and Hspice.

MEMBERSHIP

Institute of Electrical and Electronics Engineers Eta Kappa Nu (IEEE-HKN) Feb 2020 - Present
The National Society of Collegiate Scholars(NSCS) May 2018 - Present